CLAIMS

1. A method comprising:

defining a phase modulation component (PMC) of a modulation symbol as an integer multiple of fundamental time units (FTU's);

defining a set of modulation symbols in which a PMC in one symbol may overlap a position of a PMC in another symbol; and

encoding data as at least one symbol of the set.

2. The method of Claim 1 wherein the PMC is defined as a rise time at the transmitter for a single amplitude transition plus a time spacer during which no transition is permitted.

3. The method of Claim 1 wherein a total number of mixed amplitude modulation (AM)/phase modulation (PM) states is given by the equation:

$$\text{Total States } (T_1) = \sum_{n=1}^{Fix(S/T)} B^n \sum_{m=1}^{n} C(n,m) * (S - n * T + 1)^m$$

where S is a symbol period;

T is the time during which a single amplitude transition may occur between edges plus the time space during which edge transitions are not permitted;

B is a number of amplitude transitions permitted per edge; and

C(n,m) is a two dimensional matrix of coefficients.

4. The method of Claim 1 wherein the total number of mixed amplitude modulation (AM)/phase modulation (PM)/Rise Time (RT) states for 2 different rise times or different length modulation objects is given by the equation:

Total States (T_1,T_2) =

$$\sum_{n_1=1}^{Fix(S/T_1)} \quad \sum_{n_2=1}^{Fix((S-T_1)/T_2)} B_1^{n1} B_2^{n2} ((n_1+n_2)!/(n_1!n_2!)) \sum_{m=1}^{n_1+n_2} C((n_1+n_2),m) * (S - n_1T_1 - n_2T_2 + 1)^m$$

T_i is the time during which a single amplitude transition may occur between edges plus the time space during which edge transitions are not permitted in the i^{th} modulation object;

B_i is a number of amplitude transitions permitted in the i^{th} modulation object; and

$C((n_1 + n_2),m)$ is a two dimensional matrix of coefficients

5. The method of Claim 1 wherein encoding comprises:
amplitude modulating at least one bit in the symbol.

6. The method of Claim 1 wherein encoding comprises:
rise time modulating at least one bit.

7. The method of Claim 1 wherein defining a plurality of modulation symbols comprises:
populating a symbol period of S FTUs with modulation objects (T) having a width of N FTUs; where S and N are integers.

8. The method of Claim 1 wherein defining a plurality of modulation symbols comprises:
defining a maximum number of amplitude transitions per state.

9. An apparatus comprising:
mapping logic to generate a plurality of control signals to control edge transitions in a modulation symbol; and
a plurality of delay elements coupled to a clock to ensure transition in the modulation symbol occur at integer multiples of a fundamental time unit (FTU).

10. The apparatus of Claim 9 wherein the modulation symbol has phase modulation features and amplitude modulation features.

11. The apparatus of Claim 9 wherein the modulation symbol has phase modulation features and rise time modulation features.

12. The apparatus of Claim 9 wherein modulation objects are integer multiples of the FTU.

13. The apparatus of Claim 9 wherein a modulation object is defined by a rise time plus a maximum spacer before another transition is permitted.

14. An apparatus comprising:
a slot in edge group detector to determine if a transition occurred during an edge group having a plurality of fundamental time units (FTU's);

demapping logic to extract data from the occurrence of the transition within an FTU of the edge group; and

an amplitude (AM) demodulator to identify data encoded in an amplitude level.

15. The apparatus of Claim 14 further comprising:

an edge detector to generate phase slot sized pulses responsive to an incoming signal.

16. The apparatus of Claim 14 wherein the demapping logic comprises:

an edge group to symbol converter; and

a symbol to data converter.

17. The apparatus of Claim 14 further comprising:

a form synchronization unit to synchronize an output of the AM demodulator and the demapping logic.

18. The apparatus of Claim 14 further comprising:

a clock diskew unit to center a phase demodulation eye and an amplitude demodulation eye at a center of an FTU.

19. A method comprising:

modulating data using symbols having a symbol period defined as an integer multiple of a fundamental time units (FTU), the symbol having modulation objects that are integer multiples of the FTU; and

demodulating the symbols to recover the data.

20. The method of Claim 19 further comprising:

providing a forwarded clock to receive with the symbols.

21. The method of Claim 19 wherein demodulating comprises:

recovering an embedded clock from a data stream including the symbols.

22. The method of Claim 19 further comprising:

regenerating the symbols between the modulating and demodulating without demodulating the symbols; and

repeating the symbols over a communication channel.

23. The method of Claim 19 wherein modulating comprises:

encoding a fractional bit between a plurality of modulations; and

wherein demodulating comprises recovering the bit by decoding the encoded fraction at a plurality of demodulators.

24. A system comprising:

a modulator to encode data in symbols having a symbol period that is an integer multiple of a fundamental time unit (FTU), each symbol having amplitude transition components that occur on an FTU time slot;

forwarded clock logic to mimic a delay through the modulator; and

a demodulator coupled to the modulator and forwarded clock logic to decode the data from the symbols.

25. The system of Claim 24 further comprising at least a second modulator and demodulator wherein at least one data bit may be fractionally encoded across a plurality of modulators and decoded by a plurality of demodulators.

26. The system of Claim 24 further comprising:

a regenerative repeater coupled between the modulator and the demodulator, the regenerative repeater to regenerate the symbols without demodulating the symbols.